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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,055	03/16/2004	Takuya Yasui	L8462.04109	1194

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STEVENS DAVIS MILLER & MOSHER, LLP
1615 L STREET, NW
SUITE 850
WASHINGTON, DC 20036

EXAMINER	
MERANT, GUERRIER	
ART UNIT	**PAPER NUMBER**
2117	
MAIL DATE	**DELIVERY MODE**
06/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/801,055	YASUI ET AL.	
	Examiner	Art Unit	
	Guerrier Merant	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04/02/07*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's arguments/amendment with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yamauchi (US 6, 128, 253)**, and further in view of **Okamura (US 5,521,541)**

Claims 1 and 8: **Yamauchi** substantially teaches a semiconductor integrated circuit comprising:

a plurality of flip-flop circuits *(items 105 & 106, Fig. 9)* being operated by a clock signal for normal operation during a normal operation *(see normal clock input, item 101, fig. 9, and configuring* a scan chain to be operated by a clock signal for scan during a scan test *(e.g. test clock, item 102; fig. 9)*;

a clock circuit for normal operation for transmitting said clock signal for normal operation to said flip-flop circuit *(e.g. item 101, fig. 9)*;

a clock circuit for scan for transmitting said clock signal for scan to said flip-flop *(e.g. item 102, fig. 9)* circuit. But **Yamauchi** fails to teach said clock circuit for scan has a lattice-shaped wiring portion, and supplies said clock signal for scan taken out of said lattice-shaped wiring portion to said flip-flop circuit. However, **Okamura** teaches semiconductor integrated circuit comprising a plurality of flip-flop circuits *(item 106, Fig. 2)* being operated by a clock signal for normal operation during a normal operation *(col. 3, lines 7-12)*, wherein said clock circuit for scan has a lattice-shaped wiring portion (fig. 2 shows lattice-shaped wiring portion of clock 102). Therefore, at the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to replace the scan clock of **Yamauchi** with the clock taught in **Okamura** in order to reduce clock skew even when a plurality of wiring blocks are included in the semiconductor device *(e.g. col. 1, lines 45-49*; **Okumura**).

Claim 2: **Yamauchi** and **Okamura** teach a semiconductor integrated circuit as in claim1 above, wherein the flip-flop circuits are arranged in the interior and the neighborhood region of the lattice-shaped wiring portion of the clock circuit for scan *(item 106, see fig. 2 for location; **Okamura**)*, and wherein said clock circuit for scan has a external clock input terminal for scan for inputting the clock signal for scan, inputs the clock signal for scan which is transmitted from said external clock input terminal for scan to the center of said lattice-shaped wiring portion, and takes out the clock signal for scan from a predetermined location of said lattice-shaped wiring portion, respectively, to supply it to each said flip-flop circuit *(col. 5, lines 20-32; Yamauchi)*.

Claim 3: **Yamauchi** and **Okamura** teach a semiconductor integrated circuit as in claim above 1, wherein a selector circuit is arranged to each flip-flop circuit (e.g. item 211, fig. 16; Yamauchi), and wherein said selector circuit inputs the clock signal for normal operation which is transmitted through the clock circuit for normal operation and the clock signal for scan which is transmitted through the clock circuit for scan, selects said clock signal for normal operation during the normal operation to output it to said flip-flop circuit, and selects said clock signal for scan during the scan test to output it to said flip-flop circuit *(e.g. col. 8, lines 41-57; Yamauchi).*

Claim 4: **Yamauchi** and **Okamura** teach a semiconductor integrated circuit as in claim 1 above, wherein the clock circuit for normal operation is configured so that transmission paths of the clock signal for normal operation may become in a tree-shape *(col.3, lines1-25; Okamura).*

As per claim 5: **Yamauchi** and **Okamura** teach a semiconductor integrated circuit as in claim 1 above, except for a plurality of types of clock signals for normal operation which are transmitted through the clock circuit for normal operation. However, at the time the invention was made, it would have been an obvious matter of design choice to incorporate more than one normal clock input terminals as opposed to the single one taught (item 201, fig. 15) in **Yamauchi** and **Okamura**, since such a modification would have involved a mere change in the size of a component. A change in size is generally

recognized as being within the level of ordinary skill in the art. *In re Rose, 105 USPQ 237 (CCPA 1995).*

Claims 6, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yamauchi** and **Okamura** as applied to claim 1 above, and further in view of **Mc Elvain et al. (US 2006/0095872 A1)**.

Claims 6 and 9: **Yamauchi** and **Okamura** fail to teach a power supply wiring of said driver element wider in width and has a lower resistance compared with a power supply wiring of an element which configures the clock circuit for normal operation. However, **McElvain et al.** discloses *methods and apparatuses to design an Integrated Circuit (IC) with a shielding of wires. In at least one embodiment, a shielding mesh of at least two reference voltages (e.g., power and ground) is used to reduce both the capacitive coupling and the inductive coupling in routed signal wires in IC chips (see abstract).* And *each of the subset of wires is substantially wider than the third plurality of signal wires so that the subset of wires forms a power ring that reduces the impedance in the shielding mesh caused by the window in shielding mesh [0025].* Therefore at the time of the invention, one of ordinary skill in the art would have found it obvious to use the method teaching in **McElvain et al.** in the integrated circuits of **Yamauchi** and **Okamura** in order to reduce power consuming.

Claims 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Yamauchi** and **Okamura** as applied to claim 1 above, and further in view of **Meier et al. (US 5,854,567).**

As per claim 7: **Yamauchi** and **Okamura** fail to teach a power supply voltage of said driver element is made lower than the power supply voltage of the element which configures the clock circuit for normal operation. However, **Meier et al.** discloses *a clock circuit for an integrated circuit which reduces power consumption achieved by an integrated circuit arrangement having a clock driver circuit, a first terminal of at least a last stage of the clock driver circuit being supplied with a clock supply voltage that is lower in terms of amount than a general supply voltage of the integrated circuit, whereby a second terminal of the at least one last stage of the clock driver circuit is directly connected to reference potential, and whereby a load current flows between the first and second terminal (col. 2, lines 1-23).* Therefore at the time of the invention, one of ordinary skill in the art would have been motivated to include the clock system of **Meier et al.** in the integrated circuits of **Yamauchi** and **Okamura** in order to lower power consumption and minimize testing costs.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Exr. Merant Guerrier whose telephone number is (571)

270-1066. The examiner can normally be reached Monday through Thursday from 10: 30 a.m. to 3:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis Jacques, can be reached on (571) 272-6962. Draft or Informal faxes, which will not be entered in the application, may be submitted directly to the examiner at (571) 270-2066.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Guerrier Merant
06/07/07

CYNTHIA BRITT
PRIMARY EXAMINER
6-7-07